CLAIMS

1. An arrangement for selecting the largest of a plurality of input currents and adding a further current to the selected current, the arrangement comprising: a plurality of inputs for receiving said input currents; a further input for receiving said further current; an output for delivering an output current proportional to the sum of the largest of the input currents and the further current; means for feeding each of the received input currents to the main current conducting path of a respective transistor, each of the transistors having its control electrode connected to a common point; a respective follower transistor connected between the input and the common point; a mirror transistor having its control electrode connected to the common point for producing a current whose value is related to that of the largest input current; a summing arrangement for adding the largest of the input currents or a current proportional thereto to the further current or a current proportional thereto, said summing arrangement having a first input for receiving the current from the mirror transistor, a second input for receiving the further current, and an output; and means for coupling the output of the summing arrangement to the output of the arrangement.

2. An arrangement as claimed in Claim 1 in which the transistors are field effect transistors.

3. An arrangement as claimed in Claim 1 or Claim 2 including indication means for indicating which of the plurality of inputs is the largest.

4. An arrangement as claimed in Claim 3 in which the plurality is two wherein the inputs are connected to respective inputs of a comparator whose output indicates which of the inputs is the larger.

5. An arrangement as claimed in any preceding claim including a current sensing and reproduction arrangement coupled between the output of the summing arrangement and the output of the arrangement.

6. An arrangement as claimed in Claim 5 in which the output of the summing arrangement is sensed and stored in one sample period and reproduced in a subsequent sample period.

7. An arrangement as claimed in Claim 6 in which the current sensing and reproduction arrangement comprises an input coupled to a first diode connected field effect transistor, a second field effect transistor, a capacitor connected across the diode connected transistor via a first switch, means for feeding the output of the summing arrangement to the input, a second switch connected between the capacitor and the gate electrode of the second transistor, and an output coupled to the drain electrode of the second transistor, wherein the first switch is closed during the one sample period and the second switch is closed during the subsequent sample period.

8. An arrangement as claimed in Claim 7 in which the dimensions of the first and second transistors are chosen so that the current reproduced by the second transistor is less than that sensed by the first transistor by a desired factor.

9. An arrangement as claimed in Claim 7 or Claim 8 comprising a second capacitor connected across the first transistor via a third switch and a fourth switch connected between the second capacitor and the gate electrode of the second transistor wherein the third switch is closed during the subsequent sample period and the fourth switch is closed during the one sample period.

10. An arrangement as claimed in any of Claims 5 to 7 or in Claim 9 when dependent on Claim 7 comprising a comparator for determining when

the largest of the input currents is greater than a predetermined value and producing an output indicative thereof and means for subtracting the predetermined value from the output current.

11. A plurality of arrangements as claimed in Claim 10 wherein the comparator outputs are connected to respective inputs of a logic arrangement which produces an output to cause the subtracting means to be operative only when the largest input current to all the plurality of arrangements is greater than the predetermined value.

12. An arrangement as claimed in any of Claims 7 to 11 in comprising a third transistor having its gate electrode connected to the gate electrode of the second transistor and its drain electrode connected to a second output of the arrangement.

13. An arrangement for selecting the largest of a plurality of input currents and adding a further current to the selected current, the arrangement being substantially as described herein with reference to Figure 8 of the accompanying drawings.

14. A Viterbi decoder comprising a trellis network interconnecting a plurality of arrangements as claimed in any preceding claim, the plurality of inputs to each of the arrangements being derived from outputs of one or more of the arrangements as defined by the connection trellis, a corresponding plurality of probability signal generators for generating a probability signal indicating the probability that a received signal corresponds to a valid signal value, the outputs of the probability signal generators being fed to the respective further inputs of the arrangements, wherein at least one of the arrangements includes indicating means for indicating which of the plurality of inputs is the largest and the indicating means is connected to a serial in serial out shift register whose output provides the decoded data.

15. A Viterbi decoder substantially as described herein with reference to the accompanying drawings.

16. Any novel feature or any novel combination of features disclosed herein either explicitly or implicitly whether or not it relates to the same invention as that claimed in any preceding claim.